WHAT IS CLAIMED IS:

5   1.   A   signal   processing   system   having   a   variable frequency input clock comprising:

phase   detection   means   for   generating   an   error   signal representing phase difference between said variable frequency input clock and a first clock,

filtering   means   coupled   to   said   phase   detection   means   for 10   filtering said error signal,

a   numerically   controlled   oscillator,   responsive   to   said filtered   error   signal   and   a   sample   clock   for   providing   said first clock; and

buffering   means   for   receiving   an   input   signal   at   the 15   variable   frequency   input   clock   and   responsive   to   said   first clock, outputting a data signal at said first clock.

2.   The   signal   processing   system   of   claim   1   further comprising   interpolation   means   coupled   to   the   buffer   means, 20   wherein   said   interpolation   means   is   responsive   to   a   phase offset   signal   representing   an   offset   in   phase   between   the sample clock and the first clock.

3.   The   signal   processing   system   of   claim   2   further 25   comprising a modulation means for modulating the interpolated signal with a trigonometric signal having a carrier frequency to form a modulated signal.

4.   The   signal   processing   system   of   claim   3   further 30   comprising a digital to analog converter for converting said modulated signal to an analog signal.

5.   A signal processing system comprising:

means   for   providing   a   first   clock   at   a   first   clock

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frequency as a function of a sample clock having a sample clock frequency and a variable frequency input clock;

5   buffering means for receiving an input signal at the variable frequency input clock and, responsive to said first clock, outputting a data signal at said first clock frequency; and

interpolation means, responsive to a phase offset signal, 10   representing an offset in phase between the sample clock and the first clock, coupled to the output of the buffering means for providing an interpolated signal at the sample clock frequency.

15   6.   The signal processing system of claim 5 wherein the interpolation means interpolates the data signal by a non-integer value.

7.   The signal processing system of claim 5 wherein the 20   interpolation means interpolates the data signal by an integer value.

8.   The signal processing system of claim 5 further comprising modulation means for modulating the interpolated 25   signal with a trigonometric signal having a carrier frequency to form a modulated signal.

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